Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **V OUT**
2. **V +**
3. **INPUT –**
4. **INPUT +**
5. **V -**

**.019”**

**1 5 4**

**2**

**3**

**MASK**

**REF**

**.018”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .003”**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .018” X .019” DATE: 1/11/17**

**MFG: TEXAS / NSC THICKNESS .009” P/N: LMV7239**

**DG 10.1.2**

#### Rev B, 7/1